Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.004”**

**.003”**

**.004”**

**.021”**

**.021”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .004” X .003” min.**

**Backside Potential: Gate**

**Mask Ref:**

**APPROVED BY: DK DIE SIZE .021” X .021” DATE: 10/20/21**

**MFG: SILICONIX THICKNESS .009” P/N: 2N4393**

**DG 10.1.2**

#### Rev B, 7/19/02